FIG. 1(A)

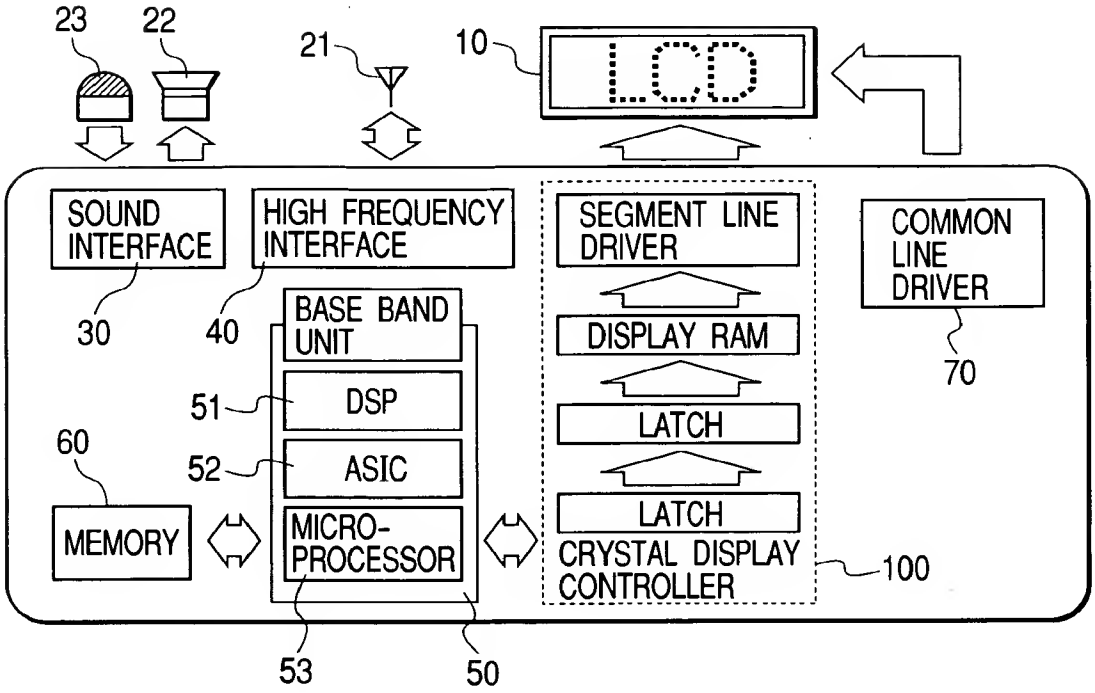

23
22
21
10
LCD
SOUND INTERFACE
HIGH FREQUENCY INTERFACE
SEGMENT LINE DRIVER
COMMON LINE DRIVER
30
40
BASE BAND UNIT
DISPLAY RAM
70
51
DSP
LATCH
60
52
ASIC
LATCH
MEMORY
MICRO-PROCESSOR
CRYSTAL DISPLAY CONTROLLER
100
53
50

FIG. 1(B)

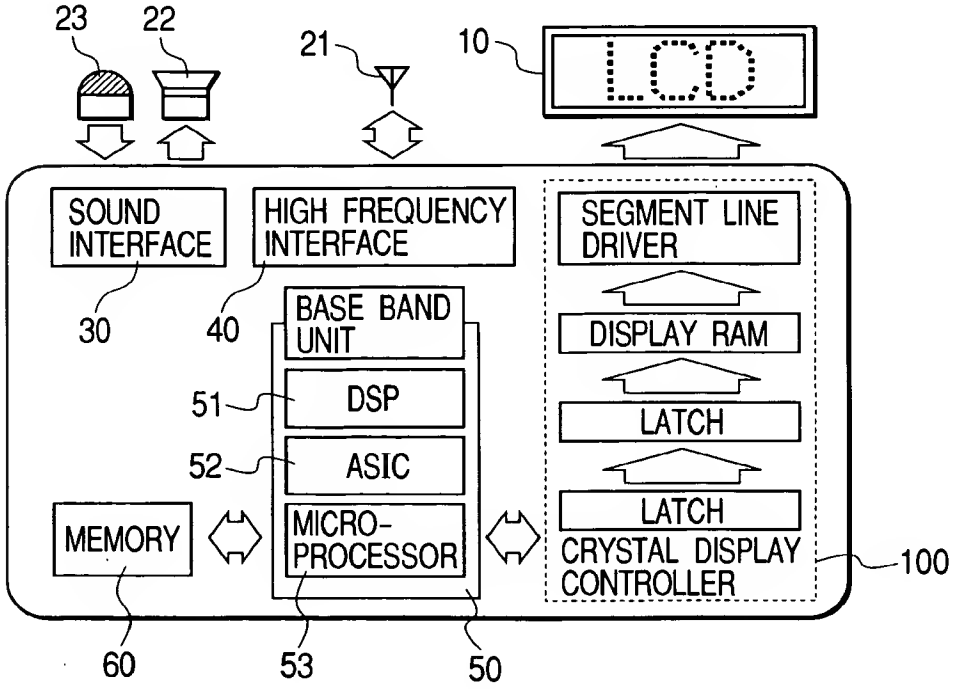

23
22
21
10
LCD
SOUND INTERFACE
HIGH FREQUENCY INTERFACE
SEGMENT LINE DRIVER
30
40
BASE BAND UNIT
DISPLAY RAM
51
DSP
LATCH
52
ASIC
LATCH
MEMORY
MICRO-PROCESSOR
CRYSTAL DISPLAY CONTROLLER
100
60
53
50

FIG. 2

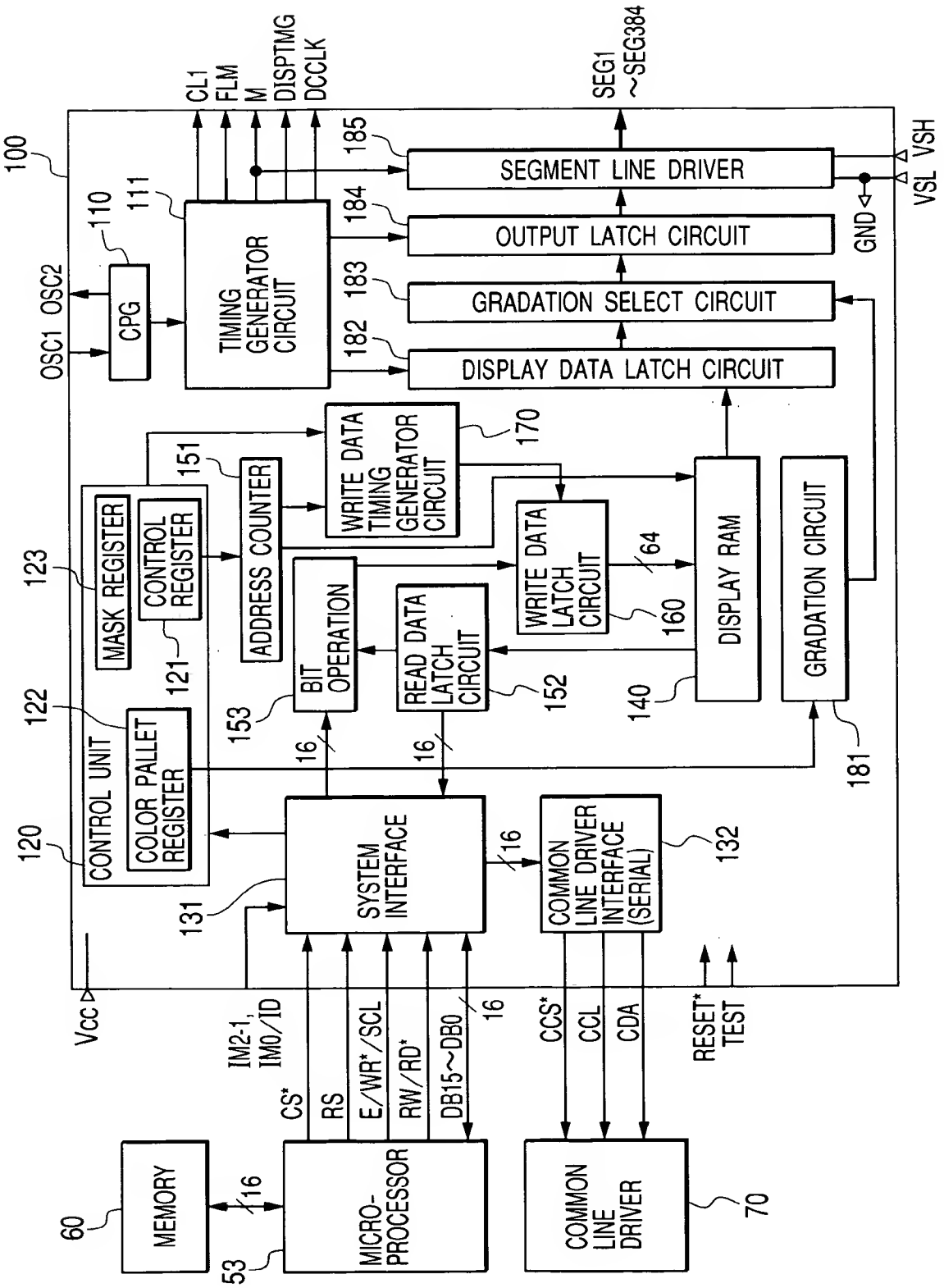

100
CL1
FLM
M
DISPTMG
DCCLK
SEG1
~SEG384
185
SEGMENT LINE DRIVER
VSL VSH
GND
184
OUTPUT LATCH CIRCUIT
183
GRADATION SELECT CIRCUIT
182
DISPLAY DATA LATCH CIRCUIT
110
111
OSC1 OSC2
CPG
TIMING GENERATOR CIRCUIT
170
WRITE DATA TIMING GENERATOR CIRCUIT
151
ADDRESS COUNTER
123
MASK REGISTER
CONTROL REGISTER
121
122
CONTROL UNIT
COLOR PALLET REGISTER
153
BIT OPERATION
READ DATA LATCH CIRCUIT
152
WRITE DATA LATCH CIRCUIT
160
64
DISPLAY RAM
140
GRADATION CIRCUIT
181
16
16
120
131
SYSTEM INTERFACE
16
COMMON LINE DRIVER INTERFACE (SERIAL)
132
Vcc
IM2-1, IM0/ID
CS*
RS
E/WR*/SCL
RW/RD*
DB15~DB0
16
CCS*
CCL
CDA
RESET*
TEST
60
MEMORY
16
53
MICRO-PROCESSOR
COMMON LINE DRIVER
70

FIG. 3

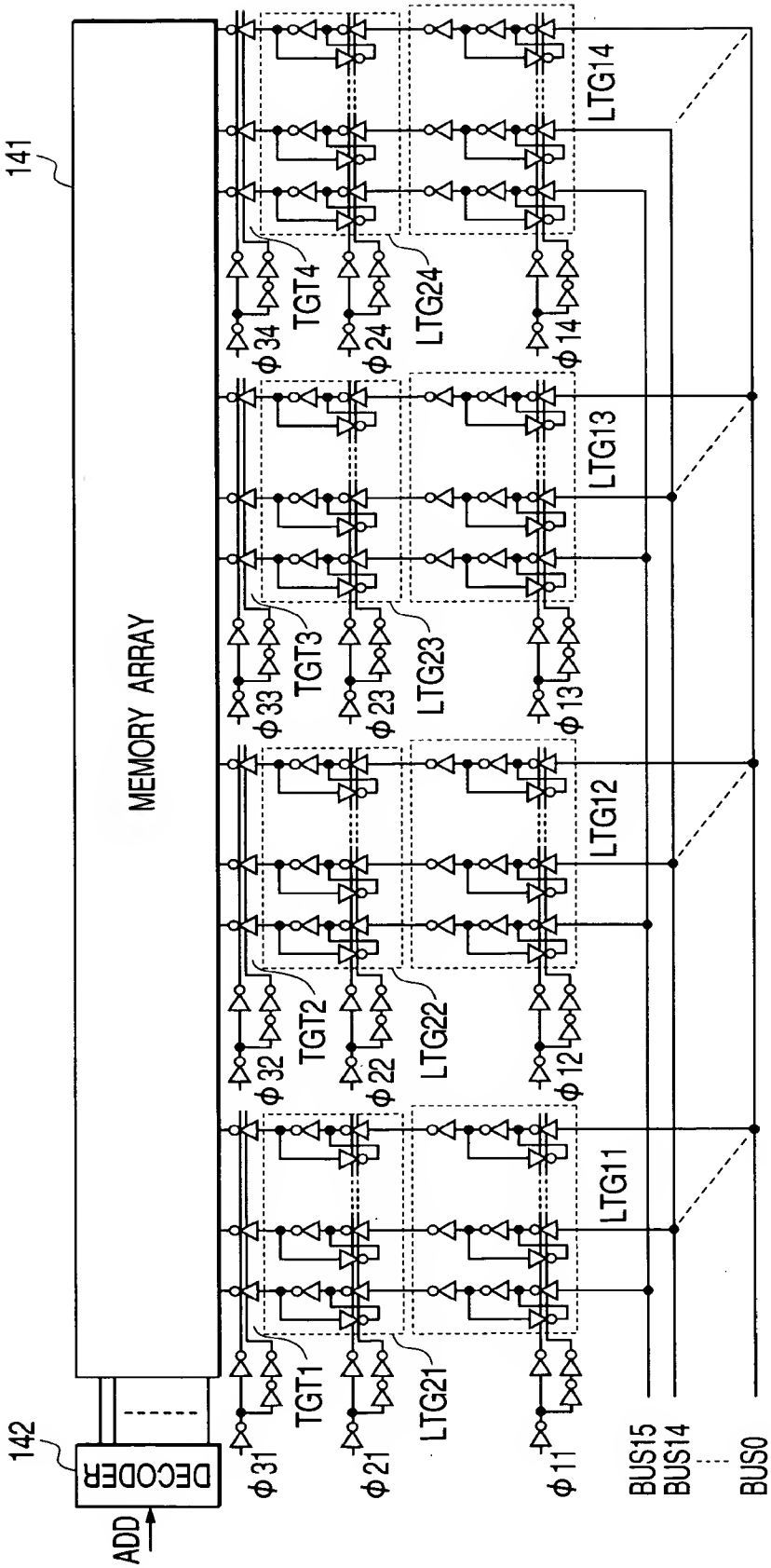

141
MEMORY ARRAY
142
DECODER
ADD
LTG14
LTG13
LTG12
LTG11
LTG24
LTG23
LTG22
LTG21
TGT4
TGT3
TGT2
TGT1
φ34
φ24
φ14
φ33
φ23
φ13
φ32
φ22
φ12
φ31
φ21
φ11
BUS15
BUS14
BUS0

FIG. 4

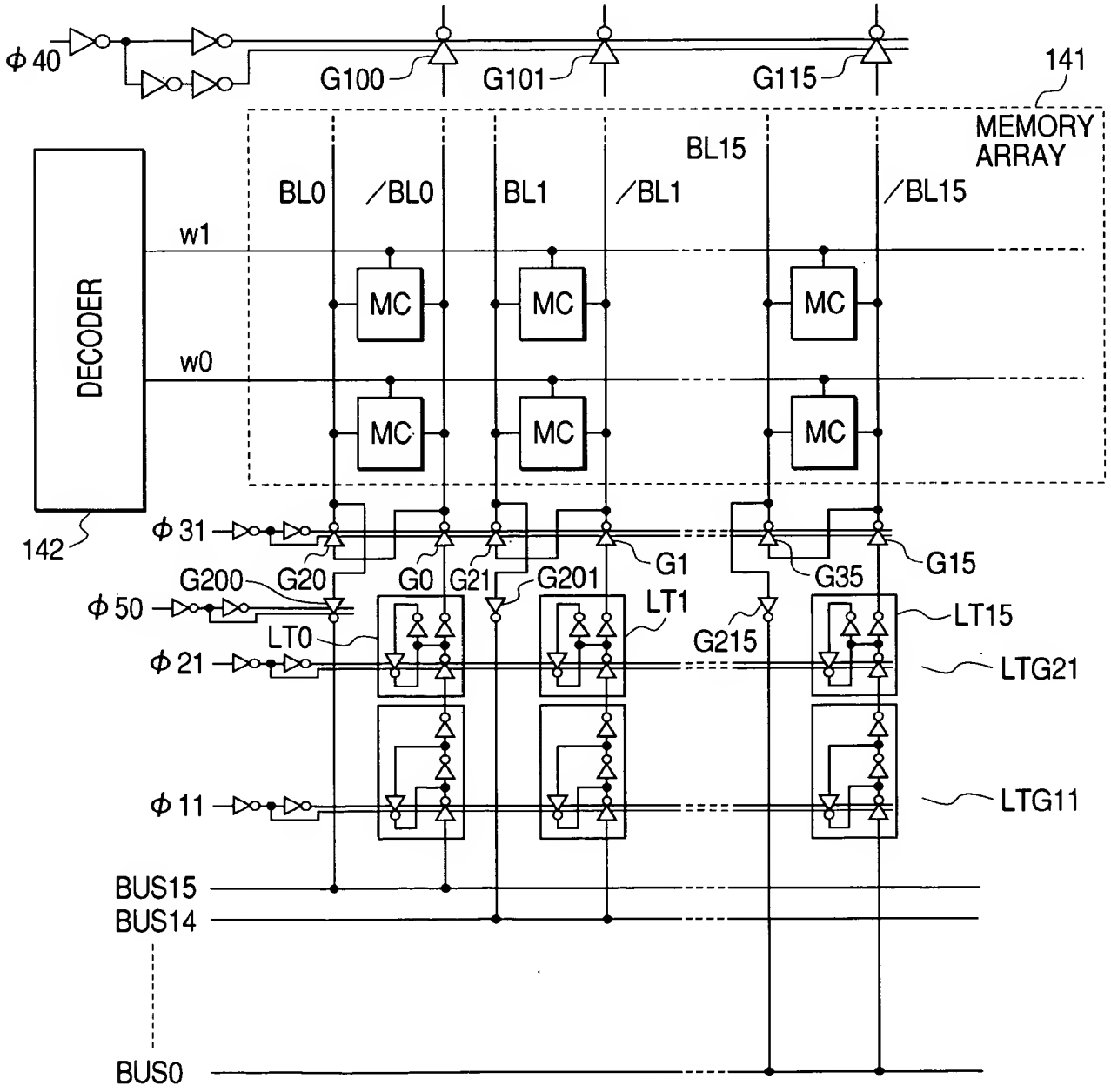

φ40
G100
G101
G115
141
MEMORY ARRAY
BL15
BL0
/BL0
BL1
/BL1
/BL15
DECODER
w1
w0
MC
142
φ31
G200
G20
G0
G21
G201
G1
G35
G15
φ50
LT0
LT1
G215
LT15
φ21
LTG21
φ11
LTG11
BUS15
BUS14
BUS0

FIG. 5(A)

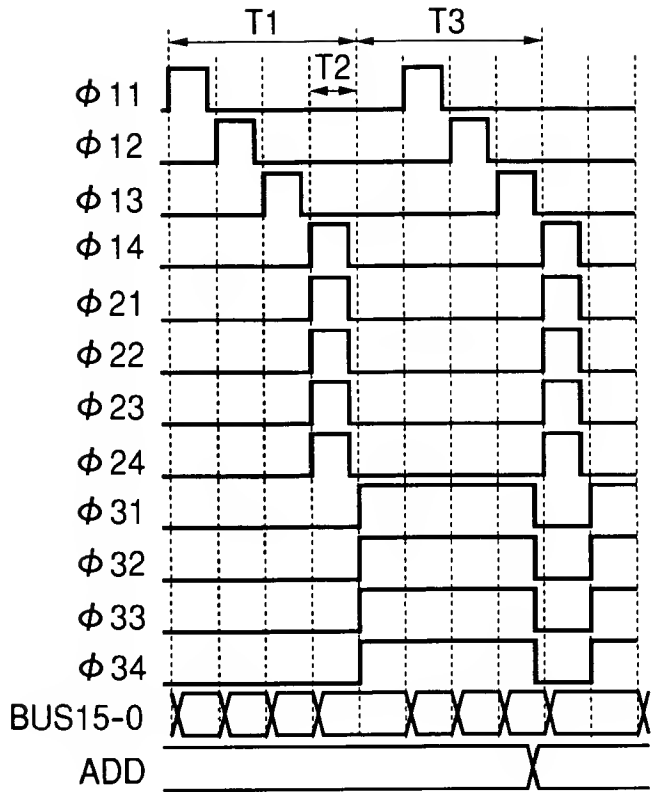

T1
T3
T2
Φ11
Φ12
Φ13
Φ14
Φ21
Φ22
Φ23
Φ24
Φ31
Φ32
Φ33
Φ34
BUS15-0
ADD

FIG. 5(B)

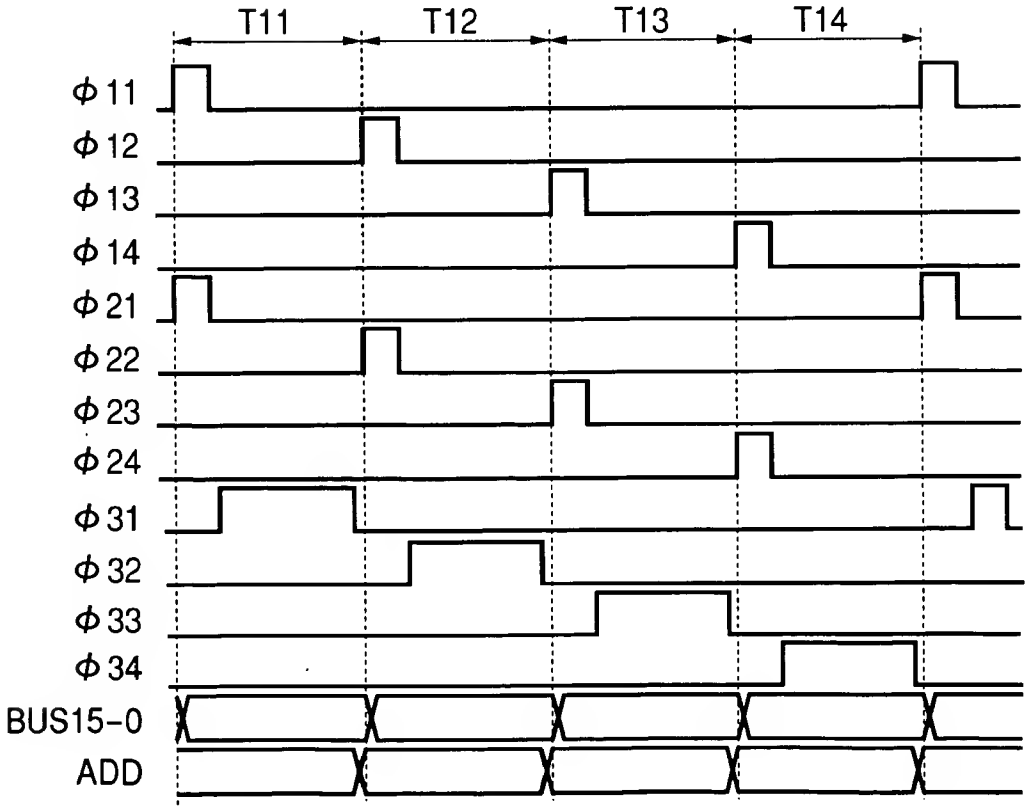

T11
T12
T13
T14
Φ11
Φ12
Φ13
Φ14
Φ21
Φ22
Φ23
Φ24
Φ31
Φ32
Φ33
Φ34
BUS15-0
ADD

FIG. 6(A)

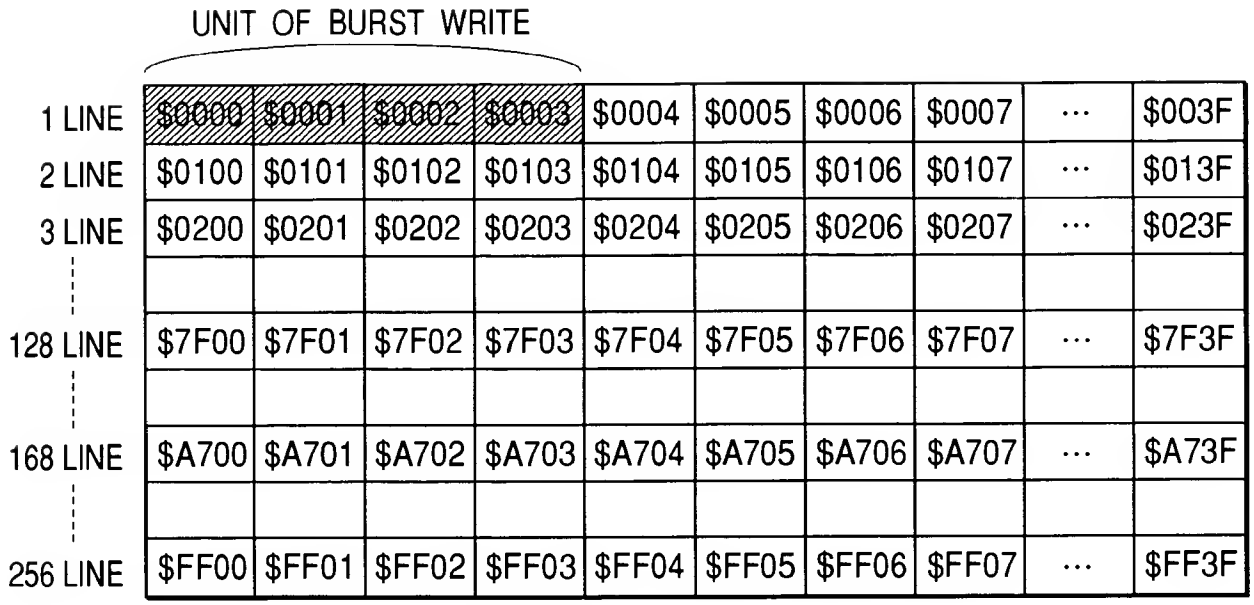

UNIT OF BURST WRITE
1 LINE
2 LINE
3 LINE
128 LINE
168 LINE
256 LINE
$0000 $0001 $0002 $0003 $0004 $0005 $0006 $0007 ··· $003F
$0100 $0101 $0102 $0103 $0104 $0105 $0106 $0107 ··· $013F
$0200 $0201 $0202 $0203 $0204 $0205 $0206 $0207 ··· $023F
$7F00 $7F01 $7F02 $7F03 $7F04 $7F05 $7F06 $7F07 ··· $7F3F
$A700 $A701 $A702 $A703 $A704 $A705 $A706 $A707 ··· $A73F
$FF00 $FF01 $FF02 $FF03 $FF04 $FF05 $FF06 $FF07 ··· $FF3F

FIG. 6(B)

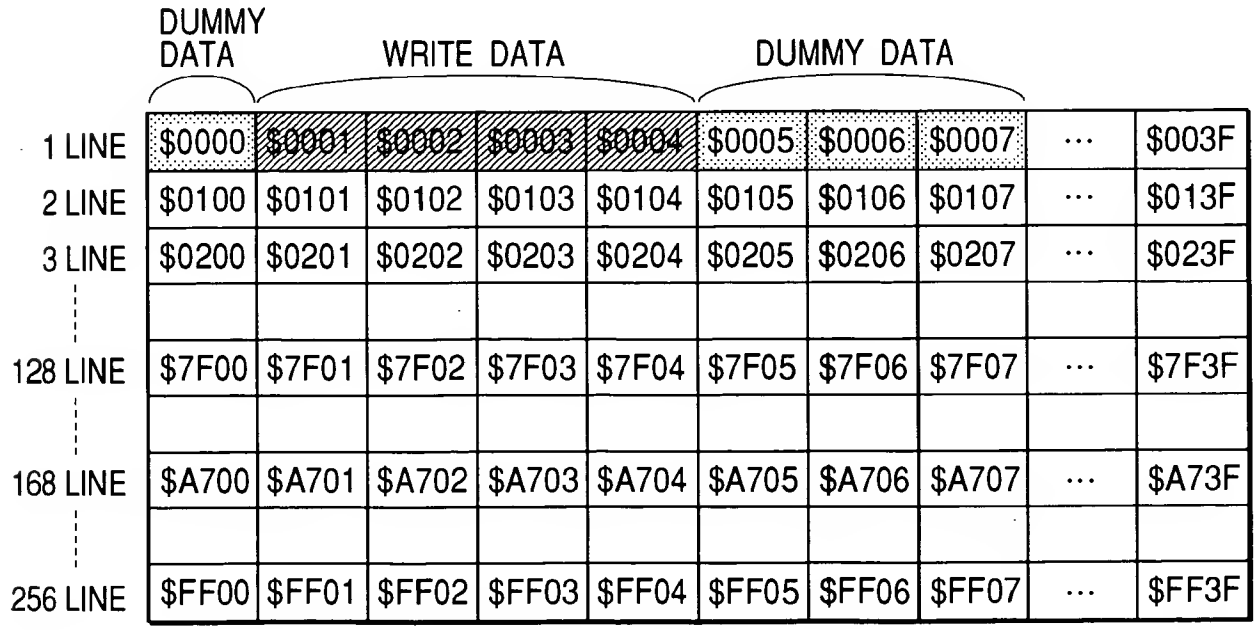

DUMMY DATA
WRITE DATA
DUMMY DATA
1 LINE
2 LINE
3 LINE
128 LINE
168 LINE
256 LINE
$0000 $0001 $0002 $0003 $0004 $0005 $0006 $0007 ··· $003F
$0100 $0101 $0102 $0103 $0104 $0105 $0106 $0107 ··· $013F
$0200 $0201 $0202 $0203 $0204 $0205 $0206 $0207 ··· $023F
$7F00 $7F01 $7F02 $7F03 $7F04 $7F05 $7F06 $7F07 ··· $7F3F
$A700 $A701 $A702 $A703 $A704 $A705 $A706 $A707 ··· $A73F
$FF00 $FF01 $FF02 $FF03 $FF04 $FF05 $FF06 $FF07 ··· $FF3F

FIG. 7(A)

i) REWRITE AREA: IN NEW 4 WORDS WRITING, A WRITE ADDRESS BEGINS FROM THE MULTIPLE OF 4.

$0000	*$0001*	*$0002*	*$0003*	$0004	$0005	$0006	$0007
$0100	$0101	$0102	$0103	$0104	$0105	$0106	$0107
$0200	$0201	$0202	$0203	$0204	$0205	$0206	$0207

NUMBER OF TIMES FOR WRITING TO LATCHES : 4 TIMES

(1)	(2)	(3)	(4)				

RAM: ONCE

FIG. 7(B)

ii) REWRITE AREA: IN NEW 8 WORDS WRITING, A WRITE ADDRESS BEGINS FROM THE MULTIPLE OF 4.

$0000	*$0001*	*$0002*	*$0003*	*$0004*	*$0005*	*$0006*	*$0007*
$0100	$0101	$0102	$0103	$0104	$0105	$0106	$0107
$0200	$0201	$0202	$0203	$0204	$0205	$0206	$0207

NUMBER OF TIMES FOR WRITING TO LATCHES : 8 TIMES

(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

RAM: TWICE

FIG. 7(C)

iii) REWRITE AREA: WHEN IT WRITES IN A DIFFERENT LINE EVERY 4 WORDS, EACH WRITE ADDRESS BEGINS FROM THE MULTIPLE OF 4.

$0000	*$0001*	*$0002*	*$0003*	$0004	$0005	$0006	$0007
$0100	*$0101*	*$0102*	*$0103*	$0104	$0105	$0106	$0107
$0200	$0201	$0202	$0203	$0204	$0205	$0206	$0207

NUMBER OF TIMES FOR WRITING TO LATCHES : 8 TIMES

(1)	(2)	(3)	(4)				
(5)	(6)	(7)	(8)				

RAM: TWICE

FIG. 8(A)

i) REWRITE AREA : IN NEW 3 WORDS WRITING, A WRITE ADDRESS DOES NOT BEGIN FROM THE MULTIPLE OF 4.

$0000	*$0001*	*$0002*	*$0003*	$0004	$0005	$0006	$0007
$0100	*$0101*	*$0102*	*$0103*	$0104	$0105	$0106	$0107
$0200	$0201	$0202	$0203	$0204	$0205	$0206	$0207

NUMBER OF TIMES FOR WRITING TO LATCHES : 4 TIMES

(1)	(2)	(3)	(4)				

RAM

ONCE

FIG. 8(B)

ii) REWRITE AREA : IN NEW 4 WORDS WRITING, A WRITE ADDRESS DOES NOT BEGIN FROM THE MULTIPLE OF 4.

$0000	*$0001*	*$0002*	*$0003*	*$0004*	*$0005*	*$0006*	*$0007*
$0100	$0101	$0102	$0103	$0104	$0105	$0106	$0107
$0200	$0201	$0202	$0203	$0204	$0205	$0206	$0207

NUMBER OF TIMES FOR WRITING TO LATCHES : 8 TIMES

(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

RAM

TWICE

FIG. 8(C)

iii) REWRITE AREA : WHEN IT WRITES IN A DIFFERENT LINE EVERY 6 WORDS, EACH WRITE ADDRESS DOES NOT BEGIN FROM THE MULTIPLE OF 4.

$0000	*$0001*	*$0002*	*$0003*	*$0004*	*$0005*	*$0006*	*$0007*
$0100	*$0101*	*$0102*	*$0103*	*$0104*	*$0105*	*$0106*	*$0107*
$0200	$0201	$0202	$0203	$0204	$0205	$0206	$0207

NUMBER OF TIMES FOR WRITING TO LATCHES : 16 TIMES

(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)

RAM

4 TIMES

FIG. 9(A)

WRITE START ADDRESS	MASK AMOUNT FOR START SIDE	WRITE END ADDRESS	MASK AMOUNT FOR END SIDE
WSA	SMW	WEA	EMW

FIG. 9(B)

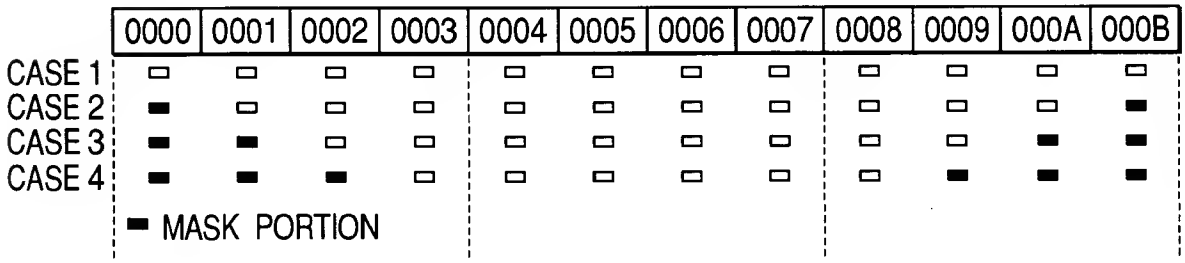


FIG. 9(C)

	WSA	SMW	WEA	EMW
CASE 1	0000	00	000B	00
CASE 2	0001	01	000A	01
CASE 3	0010	10	0009	10
CASE 4	0011	11	0008	11

FIG. 10(A)

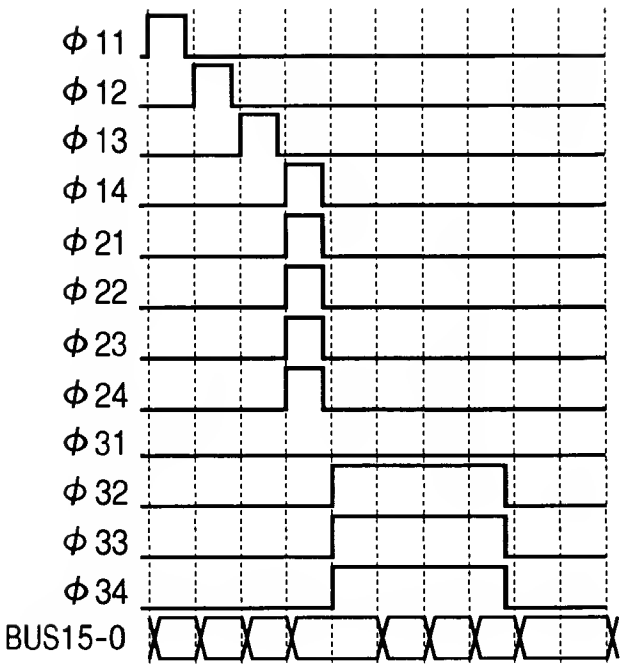


FIG. 10(B)

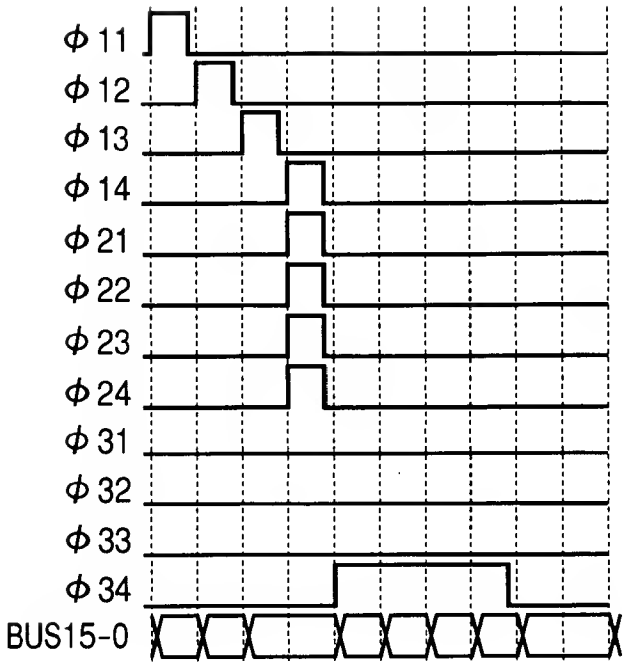


FIG. 10(C)

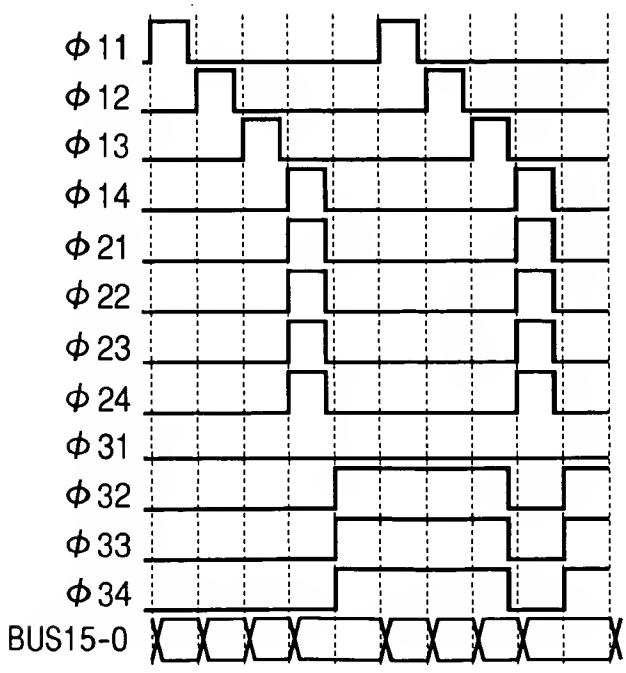


FIG. 10(D)

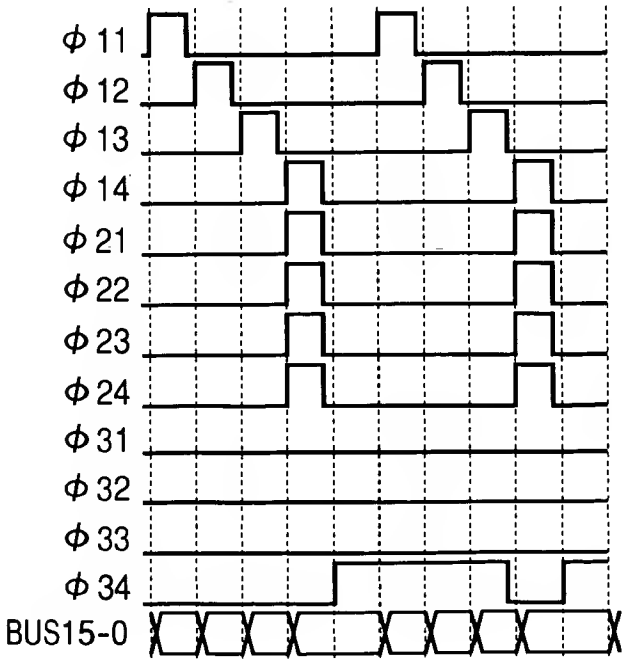
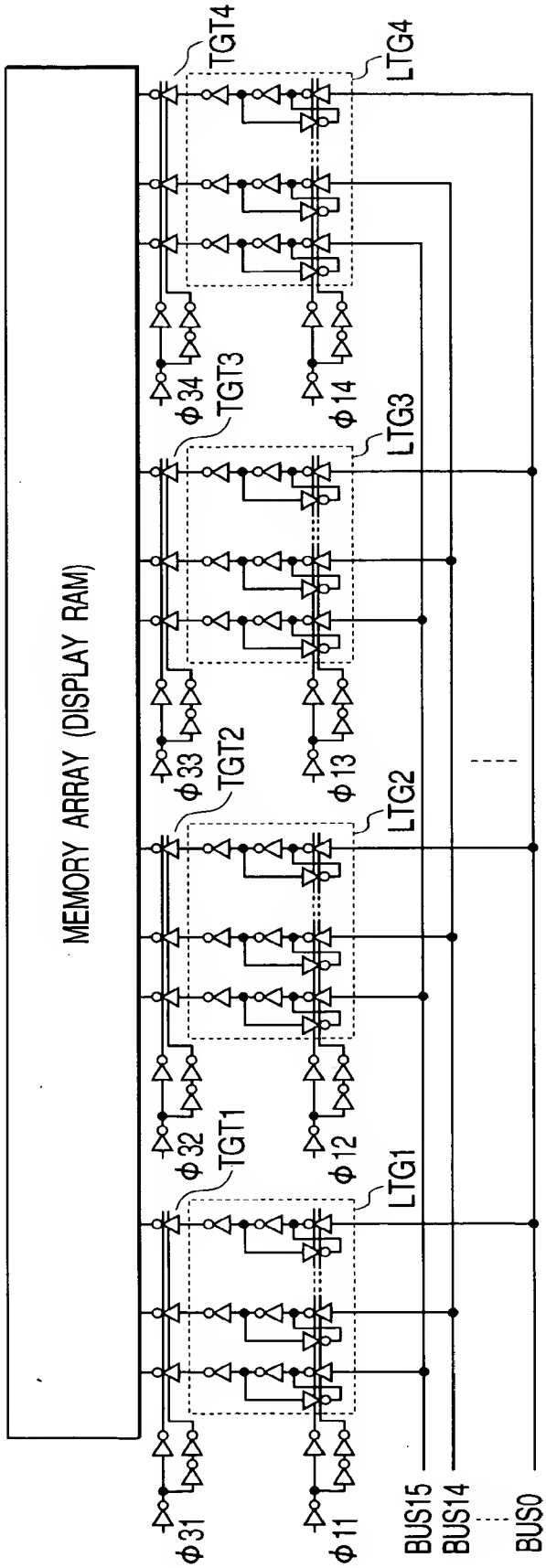


FIG. 11


MEMORY ARRAY (DISPLAY RAM)
TGT4
LTG4
TGT3
LTG3
TGT2
LTG2
TGT1
LTG1
φ34
φ14
φ33
φ13
φ32
φ12
φ31
φ11
BUS15
BUS14
BUS0

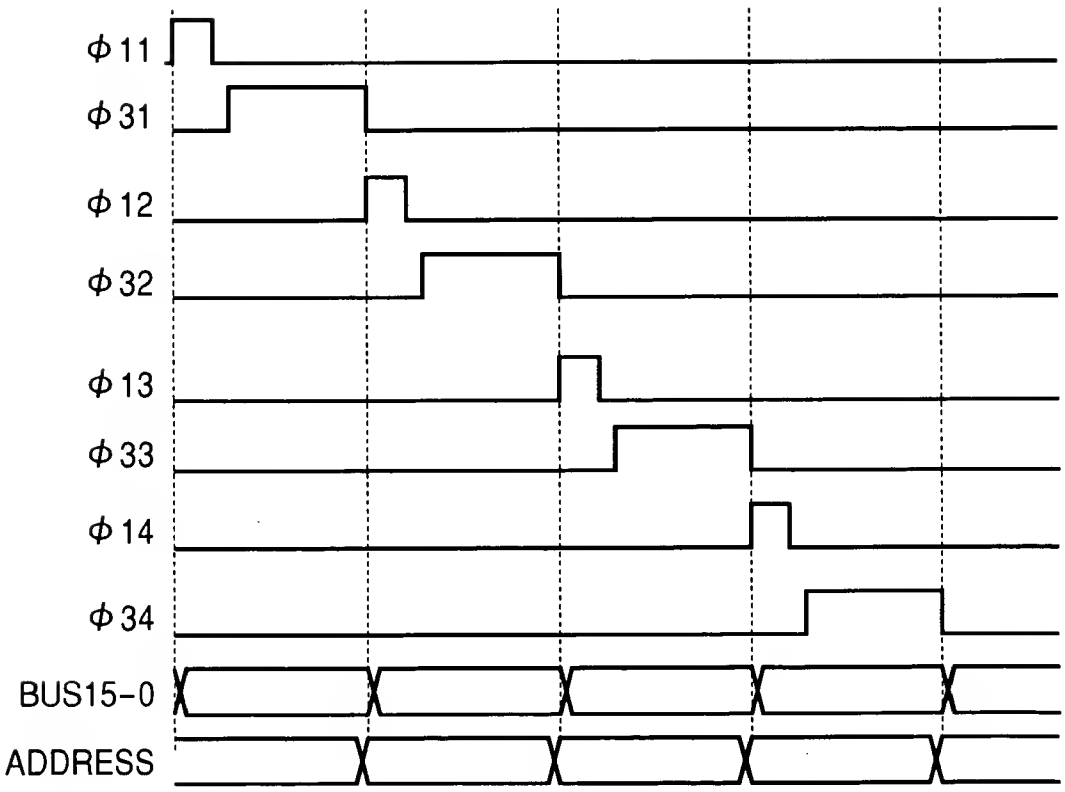



FIG. 12